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System and a method for checking lock step consistency between an in circuit ...

C Nemecek - US Patent 6,922,821, 2005 - Google Patents

... along with circuitry to provide interfacing to the base station and the device under test (DUT). ... when the system is not emulating), or when system encounters a breakpoint (eg, **sleep**, **stall**, 5 internal ...

A **clock** portion 246 carries a data **clock** plus the microcon- troller **clock** signal for ...

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### In-circuit emulator with gatekeeper based halt control

C Nemecek, S Roe - US Patent 7,236,921, 2007 - Google Patents

... If the microcontroller is not in a **sleep** mode, the gatekeeper simply queues a halt ... CYPD-CD00186;

## "Method for Breaking Execution of Test Code in a DUT and Emulator Chip ... AND DATA1 LINES

TO LOGIC HIGH 840 836 GATEKEEPER DETECTS NO **CLOCK** + DATA0 AND ...

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### In-circuit emulator with gatekeeper for watchdog timer

C Nemecek, S Roe - US Patent 7.162,410, 2007 - Google Patents

... 717/124 Steve Roe, Woodinville, WA (US) 6,922,821 R1 \* 7/2005 Nemecek 716/4 (73) Assignee:

**Cypress Semiconductor** Corporation, 6.957.180 R1 \* 10/2005 Nemecek .... The gatekeeper operates with its own gatekeeper **clock** independent of the microcontroller **clock**. ...

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BUTL TRACTION - Interface. 2010 · [eproductalert.com](http://eproductalert.com)

... Chapa also has held various management positions at Mosel/Vitelic Semiconductor,

**Cypress Semiconductor**, Wyle Labs, and Xerox Corp ... When it comes to power optimization, power-synthesis tools insert **clock** gating to reduce power. ...

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### Low pin count solution using capacitance sensing matrix for keyboard architecture

L.Hua, J.XiaoPing - US Patent App. 11/440,924, 2006 - Google Patents

... CN) Correspondence Address: BLAKELY SOKOLOFF TAYLOR & ZAFMAN 1279 OAKMEAD

PARKWAY SUNNYVALE, CA 94085-4040 (73) Assignee: Cypress Semiconductor Corporation

(21 ... 3 of 14 US 2007/0273560 A1 (N O U Q M I a. 03 ^^ Internal Oscillator/ Clocks 206 1 s ...

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### Apparatus and method for detecting multiple buttons with one pin

L GuangHai - US Patent App. 11/477,179, 2006 - Google Patents

... WITH ONE PIN Publication Classification (75) Inventor: Li GuangHai, Shanghai (CN)

Correspondence Address: BLAKELY SOKOLOFF TAYLOR & ZAFMAN 1279 OAKMEAD

PARKWAY SUNNYVALE, CA 94085-4040 (73) Assignee: **Cypress Semiconductor** Corporation ( ...

### TECHNICAL FIELD

L Guanghai - freepatentsonline.com

... a Programmable System on a Chip (PSOC™) processing device, manufactured by **Cypress**

**Semiconductor** Corporation, San ... Ic) 357 in a single direction onto a device under test ("DUT")

capacitor, capacitor ... In particular, the output of comparator 353 asserts a **clock** signal F OUT ...

### Preventing unintentional activation of a sensor element of a sensing device

J Konstas - 2008 - freepatentsonline.com

... a Programmable System on a Chip (PSoC™) processing device, manufactured by **Cypress**

**Semiconductor** Corporation, San ... Ic) 357 in a single direction onto a device under test ("DUT")

capacitor, capacitor ... In particular, the output of comparator 353 asserts a **clock** signal F OUT ...

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[... lock step consistency between an in circuit emulation and a microcontroller while ...](#)

G Nemecek - US Patent 6,922,821, 2005 - Google Patents

... synchronization. Whenever the system is halted (ie, when the system is not **emulating**), or when system encounters a breakpoint (eg, **sleep**, **stall**, 5 internal start/stop, **stalls**, etc.) a consistency check may be conducted. According ...

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E Landström - liu.diva-porta1.org

... This means translation and **emulation** of com- mands and behaviour so a SATA device can be used ... In Self Test CDB Command Descriptor Block CRC Cyclic Redundancy Check DCM Digital Clock Manager DMA Direct Memory Access DUT **Device Under Test** EOF End Of ...

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MD Ciobotaru, V Buzuloiu - 2007 - cdsweb.cern.ch

... 72 3.5.1 The ATLAS ROB **emulator** . . . . . 72 3.5.2 Network **emulator** . . . . . 73 3.6 Summary . . . . . 175 B.3 GPS **clock** synchronization . . . . . 177 B.4 PCI Interface . . . . .

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BUTL TRACTION - Interface, 2010 - eproductalert.com

... Prior experience includes verification and **emulation** engineering for MIPS and a stint as verification manager for Infineon's LAN business unit. ... When it comes to power optimization, power-synthesis tools insert **clock** gating to reduce power. ...

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... and a method for checking **lock step** consistency between an in circuit **emulation** ...

C Nemecek - US Patent 6,922,821, 2005 - Google Patents

... Whenever the system is halted (ie, when the system is not **emulating**), or when system encounters a breakpoint (eg, **sleep**, stall, 5 internal start/stop, stalls, etc.) a ... A **clock** portion 246 carries a data **clock** plus the microcon- troller **clock** signal for the microcontroller 232. ...

[Cited by 1](#) - [Related articles](#) - [All 2 versions](#)Combined in-circuit **emulator** and programmer

C Nemecek, S Roe - US Patent 7,089,175, 2006 - Google Patents

... embodiments of the present invention, to the base station, the interface having a **clock** signal me ... a flow chart of a process for entering a microcontroller can be placed in a **sleep** mode so ... 1JN VRSJN 11UJN A pod assembly for use with a combined In-Circuit **Emulation** system and ...

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C Nemecek, S Roe - US Patent 7,236,921, 2007 - Google Patents

... If the microcontroller is not in a **sleep** mode, the gatekeeper simply queues a ... GATEKEEPER **CLOCK** TO VIRTUAL MICROCONTROLLER IN PLACE OF MICROCONTROLLER **CLOCK** 852 GATEKEEPER ... entitled "Host to FPGA Interface in an In-Circuit **Emulation** System", which ...

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C Nemecek, S Roe - US Patent 7,162,410, 2007 - Google Patents

... timer event has occurred in a microcontroller, the microcontroller running in **lock-step** synchronization with a ... be performed on computer memory, controller **clock** signal with a gatekeeper **clock** signal to ... the data processing arts to most effec- ning In-Circuit **Emulation** software ...

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... and a method for checking **lock step** consistency between an in circuit **emulation** ...

C Nemecek - US Patent 6,922,821, 2005 - Google Patents

... Whenever the system is halted (ie, when the system is not **emulating**), or when system encounters a breakpoint (eg, **sleep**, stall, 5 ... check as described above and if there is a mismatch of memory content or SRAM content the host device 210 will issue a "**lock step** error". ...

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C Nemecek, S Roe - US Patent 7,089,175, 2006 - Google Patents

... embodiments of the present invention, to the base station, the interface having a **clock** signal me ... a flow chart of a process for entering a microcontroller can be placed in a **sleep** mode so ... 1JN VRSJN 11UJN A pod assembly for use with a combined In-Circuit **Emulation** system and ...

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... a gatekeeper forming a portion of a virtual microcontroller that operates in **lock-step** synchronization with a ... If the microcontroller is not in a **sleep** mode, the gatekeeper simply queues a halt ... to Nemecek entitled "Host to FPGA Interface in an In-Circuit **Emulation** System", which is ...

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... timer event has occurred in a microcontroller, the microcontroller running in **lock-step** synchronization with a ... be performed on computer memory, controller **clock** signal with a gatekeeper **clock** signal to ... the data processing arts to most effective In-Circuit **Emulation** software ...

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